WHAT IS CLAIMED IS:

1. An apparatus for coordinating communications between a plurality of tightly coupled processors, comprising:

one or more generalized queues communicatively couplable to the tightly coupled processors for storing entries to be passed between the tightly coupled processors, each queue having a start location, an end location, a put pointer for indicating a next location in the queue into which an entry is to be supplied, and a get pointer for indicating a next location in the queue from which a entry is be received; and

one or more specialized registers communicatively couplable to the tightly coupled processors for assisting the tightly coupled processors in utilizing the generalized queues for interprocessor communications and adapting the generalized queues to match a current operating environment;

wherein the generalized queues and specialized registers are configurable in accordance with programs executable in the tightly coupled processors.

2. The apparatus as recited in claim 1, further comprising at least one specialized register for storing the put pointer and the get pointer of a generalized queue associated with the specialized register to assist in supplying entries into the generalized queue, receiving entries from the generalized queue, and determining whether the generalized queue is empty, full, not full, or not empty.

3. The apparatus as recited in claim 1, further comprising at least one specialized register for storing an end location of a generalized queue associated with that specialized register to dynamically adapt a size of the generalized queue to the current operating environment.

4. The apparatus as recited in claim 1, further comprising at least one specialized register for storing requests from two or more processors to reset a generalized queue being utilized to pass entries between the processors, in order to facilitate a coordinated reset of that generalized queue.

5. The apparatus as recited in claim 1, further comprising at least one specialized register for storing attention conditions from one processor destined for another processor.

6. The apparatus as recited in claim 1, further comprising at least one specialized register for storing whether the generalized queues are not empty or not full.

7. The apparatus as recited in claim 4, further comprising at least one specialized register for storing an enable indicating whether an attention condition destined for one processor will be visible to that processor.

8. The apparatus as recited in claim 4, further comprising at least one specialized register for storing an enable indicating whether an indicator of whether the generalized queue is not empty or not full destined for one processor will be visible to that processor.

9. An interface controller chip comprising the apparatus of claim 1, the one or more tightly coupled processors for providing I/O processing and physical connectivity between a host device coupled to a host bus and external data storage devices coupled to one or more storage area networks.

10. A host bus adapter (HBA) comprising the interface controller chip of claim 9, wherein the host bus is a PCI or PCI-X bus and the external data storage devices communicate over the one or more storage area networks using fibre channel (FC) protocols.

11. A server computer comprising the HBA of claim 10.

12. In a multi-processor system including a plurality of tightly coupled processors and one or more generalized queues communicatively couplable to the tightly coupled processors for storing entries to be passed between the tightly coupled processors, an apparatus for coordinating communications between the tightly coupled processors, comprising:

one or more specialized registers communicatively couplable to the tightly coupled processors and configurable in accordance with programs executable in the tightly coupled processors for

adjusting a size and location of the generalized queues to dynamically adapt the generalized queue to the current operating environment;

informing the tightly coupled processors when the generalized queues are empty, full, not empty, or not full; and

enabling attention conditions to be passed between the tightly coupled processors.

13. An apparatus for providing I/O processing and physical connectivity between a host device coupled to a host bus and external data storage devices coupled to one or more storage area networks, comprising:

a plurality of tightly coupled processors for coordinating a transfer of information between the host device and the external storage devices;

one or more generalized queues communicatively couplable to the tightly coupled processors for storing entries to be passed between the tightly coupled processors; and

one or more specialized registers communicatively couplable to the tightly coupled processors and configurable in accordance with programs executable in the tightly coupled processors for assisting the tightly coupled processors in utilizing the generalized queues for interprocessor communications and adapting the generalized queues to match a current operating environment.

14. The apparatus as recited in claim 13, wherein the tightly coupled processors are programmed for utilizing the one or more specialized registers to:

adjust a size and location of the generalized queues to dynamically adapt the generalized queue to the current operating environment;

inform the tightly coupled processors when the generalized queues are empty, full, not empty, or not full; and

enable attention conditions to be passed between the tightly coupled processors.

15. A method for coordinating communications between a plurality of tightly coupled processors, comprising:

configuring one or more specialized registers to assist the tightly coupled processors in adapting and utilizing one or more generalized queues for storing and passing entries between the tightly coupled processors and facilitating interprocessor communications;

storing and retrieving information in the configured specialized registers for use in adapting the generalized queues to match a current operating environment;

storing and retrieving information in the configured specialized registers for use in determining when entries may be supplied into or received from the generalized queues; and

storing and retrieving attention conditions in the configured specialized registers to be passed between the tightly coupled processors.

16. The method as recited in claim 15, wherein for each generalized queue, the method further comprises storing, in the configured specialized registers, a put pointer for indicating a next location in the queue into which an entry is to be supplied and a get pointer for indicating a next location in the queue from which a entry is be received, the get and put pointers for assisting in supplying entries into the generalized queue, receiving entries from the generalized queue, and determining whether the generalized queue is empty, full, not full, or not empty.

17. The method as recited in claim 15, wherein for each generalized queue, the method further comprises storing, in the configured specialized registers, an end location of the generalized queue for dynamically adapting a size of the generalized queue to the current operating environment.

18. The method as recited in claim 17, wherein for each generalized queue, the method further comprises storing, in the configured specialized registers, requests from two or more processors to reset the generalized queue in order to facilitate a coordinated reset of that generalized queue.

19. The method as recited in claim 18, further comprising changing the size of a generalized queue by performing a coordinated reset of the generalized queue and storing a new end location in the configured specialized registers.

20. The method as recited in claim 15, further comprising storing, in the configured specialized registers, attention conditions from one processor destined for another processor.

21. The method as recited in claim 15, further comprising storing, in the configured specialized registers, whether the generalized queues are not empty or not full.

22. The method as recited in claim 15, further comprising storing, in the configured specialized registers, an enable indicating whether an attention condition destined for one processor will be visible to that processor.

23. The method as recited in claim 15, further comprising storing, in the configured specialized register, an enable indicating whether an indicator of whether the generalized queue is not empty or not full destined for one processor will be visible to that processor.

24. In a multi-processor system including a plurality of tightly coupled processors and one or more generalized queues communicatively couplable to the tightly coupled processors for storing entries to be passed between the tightly coupled processors, a method for coordinating communications between the tightly coupled processors, comprising:

configuring one or more specialized registers to assist the tightly coupled processors in adapting and utilizing the generalized queues for storing and passing entries between the tightly coupled processors and facilitating interprocessor communications;

adjusting a size and location of the generalized queues in accordance with information stored in the specialized registers to dynamically adapt the generalized queues to the current operating environment;

informing the tightly coupled processors when the generalized queues are empty, full, not empty, or not full in accordance with information stored in the specialized registers; and

passing attention conditions between the tightly coupled processors in accordance with information stored in the specialized registers.